Amend the ABSTRACT OF THE DISCLOSURE on page 19 with the following replacement ABSTRACT OF THE DISCLOSURE.

A method and apparatus for reducing logic activity in a microprocessor which examines every instruction before it is executed and determines in advance the minimum appropriate datapath width (in byte or half-word quantities) necessary to accurately execute the operation. Achieving this requires two major enhancements to a traditional microprocessor pipeline. First, extra logic (potentially an extra pipeline stage for determining an operation's effective bit width -the WD width detection logic) is introduced between the Decode and Execution stages. Second, the traditional Execution stage architecture (consisting of the register file RF and the arithmetic logical unit ALU), instead of being organized as one continuous 32-bit unit, is organized as a collection of multiple slices, where a slice can be of an 8-bit (a byte) or a 16-bit (double byte) granularity. Each slice in this case can operate independently of each other slice, and consists of a portion of the register file, functional unit and cache memory. Concatenating a multiple number of these slices together creates a required full width processor. ~~These slices work either all in parallel when a full-width operation is executed, or only the lowermost slice(s) is (are) (minimum required number) enabled for the case of narrow-width operations. Slices are enabled on a cycle-by-cycle basis by the width determination logic using information on RF value widths and signs which are stored for each register value. The WD logic achieves the enablement of various slices through the use of clock gating.~~